Listing of Claims:

1. (Previously presented) A method comprising:
storing incoming frames of digital television data in a first frame buffer of an interface logic;
reading outgoing frames of digital television data from a second frame buffer of the interface logic;
monitoring a feedback signal provided by a graphics controller coupled to the system, the monitoring by the interface logic and the feedback signal indicates whether a programmed position of a display device has been refreshed; and
transmitting the outgoing frames of digital television data in the second frame buffer to the graphics controller to be displayed on the display device when the programmed position of the display device is refreshed.

2. (Previously presented) The method of claim 1, further comprising:
storing the incoming frames of digital television data in the second frame buffer;
reading the outgoing frames of digital television data from the first frame buffer; and
transmitting the outgoing frames of digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

3. (Previously presented) The method of claim 1, further comprising:
detecting whether the outgoing frames of digital television data is stored in the first frame buffer or the second frame buffer.

4. (Previously presented) The method of claim 1, the monitoring further comprising:

monitoring a horizontal sync and a vertical sync of the display device.

5. (Cancelled).

6. (Previously presented) The method of claim 1, the transmitting further comprising:

transmitting the outgoing frames of digital television data over a peripheral component interconnect (PCI) bus.

7. (Cancelled).

8. (Previously presented) A system comprising:

a central processing unit (CPU);

a graphics controller coupled to the CPU;

a local bus coupled to the CPU and graphics controller; and

digital television/local bus interface logic coupled to the graphics controller by way of the local bus, the digital television/local bus interface logic comprising:

a digital television interface that receives incoming digital television data;

a local bus interface that transmits outgoing digital television data to the graphics controller over the local bus;

a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller that stores the incoming digital television data to one frame buffer and reads the

outgoing digital television data from another frame buffer

wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.

9. (Original) The system of claim 8, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

10. (Original) The system of claim 8, further comprising:

a display device coupled to the local bus for receiving outgoing digital television data over the local bus.

11. (Previously presented) The system of claim 8, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

12. (Previously presented) The system of claim 8, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

13. (Previously presented) The system of claim 8, wherein the local bus interface monitors a refresh of the display device for receiving the outgoing digital television data.

14. (Original) The system of claim 8, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

15. (Original) The system of claim 8, the digital television/local bus logic further comprising:

a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

16. (Original) The system of claim 8, the digital television/local bus logic further comprising:

a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

17. (Previously presented) A digital television/local bus interface logic, comprising:

a digital television interface that receives incoming digital television data;

a local bus interface that transmits outgoing digital television data to a graphics controller for display on a display device;

a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh

of the display device, the first and second portions of the refresh identified by a feedback signal from a graphics controller.

18. (Original) The interface logic of claim 17, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

19. (Cancelled).

20. (Original) The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

21. (Original) The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

22. (Original) The interface logic of claim 17, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

23. (Original) The interface logic of claim 17, further comprising:

a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

24. (Original) The interface logic of claim 17, further comprising:

a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

25.-33. (Cancelled).

34. (Previously presented) A digital television data handling system, comprising:

a first means for storing incoming digital television data and outgoing digital television data in an alternating manner;

a second means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a means for monitoring a feedback signal provided by a means for controlling graphics, the feedback signal indicates whether a programmed position of a display device has been refreshed; and

a means for transmitting the outgoing digital television data in one of the means for storing to the means for controlling graphics for display on the display device when a programmed position of the display device is refreshed.

35. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for reading the outgoing digital television data from one of the means for storing.

36. (Previously presented) The system of claim 34, the means for monitoring comprising:

a means for monitoring a horizontal sync and a vertical sync of the display device.

37. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for detecting whether the outgoing digital television data is stored in the first means for storing or the second means for storing.

38. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus.

39. (Cancelled).

40. (Previously presented) A closed loop digital television data anti-tearing system, comprising:

a central processing unit (CPU);

a local bus coupled to the CPU;

a graphics controller coupled to the local bus;

a display device that receives outgoing digital television data from the graphics controller; and

a digital television/local bus interface logic coupled to the local bus that stores incoming digital television data and the outgoing digital television data and selectively provides the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed;

wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.

41. (Original) The anti-tearing system of claim 40, further comprising:

a core logic coupled between the local bus and the graphics controller.

42. (Original) The anti-tearing system of claim 40, further comprising:

a digital television decoder for providing incoming television data to the digital television/local bus interface logic.

43. (Original) The anti-tearing system of claim 42, further comprising:

a digital television tuner for providing incoming digital television data to the digital television decoder.

44. (Previously presented) A closed loop digital television data anti-tearing system, comprising:

a local bus;

a graphics controller coupled to the local bus;

a display device for receiving outgoing digital television data from the graphics controller; and

a digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed,

wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data, and wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.

45. (Original) The anti-tearing system of claim 44, wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device.

46. (Original) The anti-tearing system of claim 40, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

47. (Cancelled).

48. (Original) A dual stream digital television/local bus interface logic, comprising:

a first digital television interface for receiving a first incoming digital television data stream;

a second digital television interface for receiving a second incoming digital television data stream;

a local bus interface for transmitting a first outgoing digital data stream and a second outgoing digital television data stream;

a first frame buffer for storing the first incoming digital television data stream and the first outgoing digital television data stream in an alternating manner;

a second frame buffer for storing the first outgoing digital television data stream and the first incoming digital television data stream in an alternating manner;

a third frame buffer for storing the second incoming digital television data stream and the second outgoing digital television data stream in an alternating manner;

a fourth frame buffer for storing the second outgoing digital television data stream and the second incoming digital television data stream in an alternating manner; and

a memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the

first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and

transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device.

49. (Original) The interface logic of claim 48, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

50. (Original) The interface logic of claim 48, wherein a refresh rate of the first outgoing digital television data stream is decoupled from a refresh rate of the first incoming digital television stream and a refresh rate of the second outgoing digital television data stream is decoupled from the refresh rate of the second incoming digital television data stream.

51. (Original) The interface logic of claim 48, further comprising:

a local bus interface buffer for receiving and storing the first outgoing digital television data stream from the first frame buffer and the second frame buffer and for receiving and storing the second outgoing digital television data stream from the third frame buffer and the fourth frame buffer.

52. (Original) The interface logic of claim 48, further comprising:

a first set of digital television interface buffers coupled to the first digital television interface for receiving a first incoming digital television data stream; and

a second set of digital television interface buffers coupled to the second digital television interface for receiving the second incoming digital television data stream.